PATENT ABSTRACTS OF JAPAN

(11)Publication number : 10-173055

(43)Date of publication of application : 26.06.1998

(51)Int.Cl. H01L 21/82
G06F 17/50

(21)Application number : 08-328371

(22)Date of filing : 09.12.1996

(71)Applicant : SONY CORP

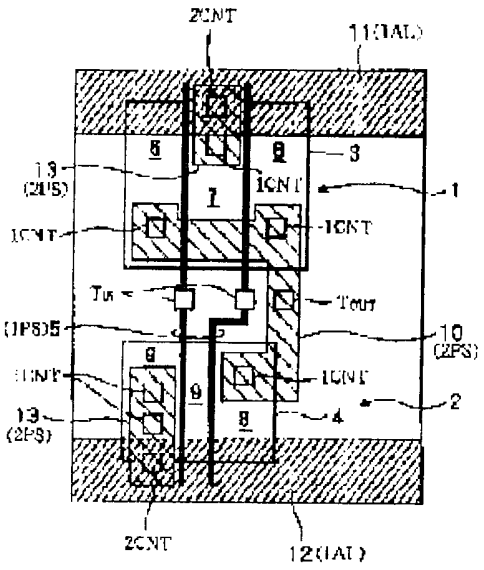
(72)Inventor : TANAKA SHUJI

(54) CELL-BASED SEMICONDUCTOR DEVICE AND STANDARD CELL

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce the cell area with ensuring a certain degree of freedom of the signal line interconnection between cells.

SOLUTION: The cell composed of combined desired circuit function blocks, including basic elements 1, 2, inner wiring 10 for internally connecting the basic elements 1, 2, and power lines 11, 12 for feeding power voltages to the elements 1, 2; the lines 11, 12 being interconnected between cells adjacent to both sides of one element. The signal line 10 is composed of a lower wiring layer than the power lines 11, 12. A not shown signal line wiring laminated above the lines 11, 12 form external signal lines wiring input/output terminals of different cells. This allows the second layer and following wiring layers to be used as power lines, the line width thereof to be reduced more than that in prior art, and the cell area to be reduced because of effective use of the lower layers of the power lines.



LEGAL STATUS

[Date of request for examination]

[Date of sending the examiner's decision of rejection]

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] this invention relates to the cell base semiconductor device which can reduction-ize cell area, and a standard cell, securing the flexibility of signal-line connection of cells to some extent.
[0002]
[Description of the Prior Art] The semi custom-made design technique of the so-called former and cell base (or it is also called a building block system) is ASIC (Application Specific Integrated Circuit). It is widely adopted as the design. By this design technique, improvement in efficiency of IC design is achieved by combining the common design property registered into the library, and using an automatic-layout wiring tool. The cell base ASIC is divided roughly into the standard cell which makes circuit functional block constitute combining the unit logical circuit (or for an element simple substance to be also good) which carried out cell registration, and the general cell method which makes a layered structure already designed circuit functional block, and carries out arrangement wiring.
[0003] Drawing 3 and drawing 4 are pattern views which illustrate the conventional unit cell which is used for the design of the cell base ASIC and is beforehand registered into the library. Drawing 3 shows the NAND cell of 2 inputs, and drawing 4 shows the NOR cell of 3 inputs. A sign 1 among drawing 3 and drawing 4 A P-channel-MOS transistor (It is hereafter called PMOS) and 2 An N channel MOS transistor p type active region and 4 (it is hereafter called NMOS) and 3 n type active region, A gate electrode and 6 5 The drain field of PMOS1 (p+ impurity diffusion field), The source field (p+ impurity diffusion field) of PMOS1 and 8 7 The drain field of NMOS2 (n+ impurity diffusion field), For 9, as for an internal signal line and 11, the source field (n+ impurity diffusion field) of NMOS2 and 10 are [a supply voltage supply line and 12] each pattern of a GND line (in this invention, 11 and 12 are named a power supply line generically).
[0004] The gate electrode 5 consists of contest polysilicon of the 1st layer (1PS), a polycide, etc. The input terminal TIN is formed in the middle of each gate electrode 5.
[0005] On the gate electrode 5, through a layer insulation layer, the laminating of the internal signal line 10 is carried out, for example, it consists of films, such as contest polysilicon of the 2nd layer (2PS), a polycide, and a tungsten. The 1st contact (1CNT) is prepared in the layer insulation layer of internal signal-line 10 ground The internal signal line 10 is connected to the drain field 6 of PMOS1, and one drain field 8 of NMOS2 through this 1CNT. In the middle of the internal signal line 10, it is an output terminal TOUT. It is prepared.
[0006] On the other hand, on the other hand, the power supply lines 11 and 12 are wired in parallel with a direction in the vertical portion of a cell, and this wiring width of face is unified between the cells from which a kind differs (this example between the NAND cell of drawing 3 , and the NOR cell of drawing 4). This is for supply voltage supply line 11 internal comrades and GND line 12 comrades to carry out a series connection only by on the other hand arranging in a direction the cell from which a kind differs. The supply voltage supply line 11 is connected to the source field of PMOS through 1CNT. Moreover,

the GND line 12 is connected to the source field 9 of another side of NMOS2 through 1CNT.
[0007] Thus, in the design of the conventional cell base ASIC using the unit cell constituted, if the required function based on customer specification, a performance, a constraint, etc. are given to an automatic-layout wiring tool, by this automatic-layout wiring tool, a suitable logical circuit cell (unit cell) will be called from a library, and the optimal pattern design will be performed. That is, after carrying out an automatic layout combining the unit cell from which a kind differs so that customer specification (a function, performance) may be fulfilled, the automatic connection of between each arranged cell is carried out by the multilayer interconnection.
[0008] For example, in the example of drawing 3 and drawing 4 , the interconnection of supply voltage supply line 11 comrades inside a cell train and the GND line 12 comrades is carried out only by carrying out an automatic layout, respectively, and they are an input/output terminal TIN and TOUT between cells by the above-mentioned automatic wiring. Wiring of the external signal line which carries out interconnection, and wiring of the external power line which communalizes the supply voltage supply line 11 of each cell train and each cell train GND line 12, respectively are performed.
[0009]
[Problem(s) to be Solved by the Invention] Since the unit cell in which the circuit or element of a predetermined function was installed beforehand constitutes various circuit functional block according to a demand of a customer as mentioned above and it is offered, in the design stage, it is required that the flexibility of wiring of connection between the cell should be large so that it can respond to any circuits. Concretely, it means that the own pattern or own node of a unit cell do not become it obstructive to connection of the next external signal line that the flexibility of wiring of connection between cells is large. For this reason, for example by drawing 3 and drawing 4 , as for both the internal signal line 10, the supply voltage supply line 11, and the GND line 12, a layer [1st] wiring layer (for example, tungsten layer) is used. Moreover, in the case of this wiring, you also have to take the problem of signal delay into consideration. That is, the proper use of a wiring layer according to the kind of signal which an obstructive thing likes as for the wiring which the signal line which connects near uses the wiring by the side of a lower layer, for example, carries a signal to long distances, such as a clock line and a bus line, of the flexibility of wiring being [that there is nothing] high, and using the wiring by the side of the low upper layer of resistance is made.
[0010] It is more desirable for flattening to become important on the other hand, if the ease of a next process is taken into consideration the more in the position of a semiconductor process the more wiring structure becomes a multilayer, for a lower layer side to make thickness thin, and for an upper layer side to thicken. in addition, the way which made the L&S (Line and Space) interval large in the field of processability, so that it went to the upper layer side more -- desirable -- moreover, the lowest layer -- a tungsten film etc. -- comparatively -- alike -- quantity -- it is obliged to use of material [****] in many cases moreover, it is comparatively alike and consists of material with high resistivity, and it is comparatively alike, and since it is thin, as an internal wiring layer which connects between adjoining elements, such as 1PS and a tungsten film, it is suitable [with the above viewpoint / this layer / 1st / wiring layer]
[0011] however, with the cell base ASIC in recent years which may take large-scale circuitry, it is because a layer [1st] wiring layer is used for the power supply line inside a cell -- it is disadvantageous -- it is becoming large relatively by the relation with flexibility reservation of wiring between cells That is, in the manufacture process of IC in recent years, by multilayering wiring structures, such as four layers and five layers, the resource of wiring increases and the flexibility of wiring is increasing with this. Moreover, with large-scale-izing and improvement in the speed of a logical circuit, the demand of the formation of area reduction or shortening of a wire length increases gradually, and supposes that almost all wiring is performed on a cell arrangement field, without preparing a wiring field between cells like [former]. however -- from [that the power supply line inside a cell is constituted from the conventional cellular structure by the layer / 1st / wiring layer with high sheet resistance] -- inevitable -- internal power supply line breadth -- large -- not taking -- it did not obtain but reduction-izing of cell area was difficult for the actual condition

[0012] this invention aims at offering the cell base semiconductor device which can reduction-ize cell area, and a standard cell, being made in view of such the actual condition, and securing the flexibility of signal-line connection of cells to some extent.
[0013]
[Means for Solving the Problem] In order to solve the trouble of the conventional technology mentioned above and to attain the above-mentioned purpose, in the cell base semiconductor device of this invention It is the cell base semiconductor device with which desired circuit functional block is constituted when a basic element combines arbitrarily at least two or more kinds of cells currently formed beforehand. The basic element of plurality [cell / aforementioned], It connects with the internal signal line to which two or more aforementioned basic elements are connected inside a cell mutually between the cells which adjoin the both sides of a direction on the other hand. It is characterized by having the power supply line which supplies supply voltage to the aforementioned basic element, for the aforementioned internal signal line being constituted from the aforementioned power supply line by the wiring layer by the side of a lower layer, and the wiring layer for signal lines by which the laminating is carried out to the upper layer side from the aforementioned power supply line constituting the external signal line which makes between the input/output terminals of a different cell connect.
[0014] Thus, in this cell base semiconductor device, by making the power supply line in a cell constitute from an internal signal line in the wiring layer by the side of the upper layer, the wiring layer after the 2nd layer which generally consists of aluminum etc. can be used as a power supply line, and line breadth of a power supply line can be made narrower than before. Moreover, since the wiring layer pattern of the 1st layer and contact can be formed in the lower layer side of a power supply line, reduction-ization of cell area becomes easy. Consequently, a power supply line will be upper-layer-ized conventionally, and the flexibility of wiring between cells falls a little in this meaning. However, as having described previously, the flexibility fall of connection between cells seldom poses a problem by making it not pull out an internal signal line outside a power supply line in consideration of the flexibility of connection between cells increasing sharply with multilayering of wiring structure in recent years, but the big effect that the cell area by upper-layer-izing of a power supply line is reduction-ized by this invention can acquire.
[0015] If it is when the cell of the same function is connected continuously, for example, the external signal line can be made to wire from a viewpoint of flexibility reservation of connection between this cell, by the same hierarchy [as a power supply line], or lower layer side, although it is desirable to use the wiring layer by the side of a lower layer as much as possible as for a power supply line. The external signal line in this case can wire flexibility satisfactory at all, if the position of an input/output terminal is determined and set so that a power supply line and abbreviation parallel may be made to wire for example.
[0016] In the standard cell of this invention, it is the standard cell which has the internal signal line to which two or more basic elements and two or more aforementioned basic elements are connected inside a cell, and the power supply line which is mutually connected between the cells which adjoin the both sides of a direction on the other hand, and supplies supply voltage to the aforementioned basic element, and the aforementioned internal signal line is characterized by consisting of aforementioned power supply lines in the wiring layer by the side of a lower layer.
[0017]
[Embodiments of the Invention] Hereafter, the cell base semiconductor device and standard cell concerning this invention are explained in detail, referring to a drawing. Drawing 1 and drawing 2 are pattern views which illustrate the unit cell (standard cell) concerning this operation gestalt which is used for the design of the cell base ASIC and is beforehand registered into the library. The standard cell of this invention has the feature in this pattern view, and when the cell base semiconductor device of this invention combines arbitrarily the cell from which a kind which is illustrated in this pattern view differs, desired circuit functional block is constituted. Therefore, by the following explanation, by explaining drawing 1 the important section of this invention is indicated to be, and the cell pattern of drawing 2 explains the operation gestalt of this invention.

[0018] Drawing 1 corresponds with drawing 3 which shows the NAND cell of 2 inputs in the cell base ASIC of this invention, and shows the conventional example. Moreover, drawing 2 corresponds with drawing 4 which shows the NOR cell of 3 inputs in the cell base ASIC of this invention, and shows the conventional example. In addition, the composition which overlaps the conventional cell shown in drawing 3 and drawing 4 here attaches the same sign, and the detailed explanation is omitted. A sign 1 NMOS and 3 for PMOS and 2 among drawing 1 and drawing 2 p type active region, 4 a gate electrode and 6 for n type active-region region and 5 The drain field of PMOS1 (p+ impurity diffusion field), The source field (p+ impurity diffusion field) of PMOS1 and 8 7 The drain field of NMOS2 (n+ impurity diffusion field), In the source field (n+ impurity diffusion field) of NMOS2, and 10, an internal signal line and 11 show a supply voltage supply line, and 12 shows [9] each pattern of a GND line (in this invention, 11 and 12 are named a power supply line generically) Moreover, Sign TIN is an input terminal and TOUT. An output terminal and 1CNT show the 1st contact (connection between the 1st wiring layer, and the source field 7 or the drain field 8 hole).

[0019] The cell of this operation gestalt differing from the case of the former of drawing 3 and drawing 4 is that the supply voltage supply line 11 and the GND line 12 are constituted from a layer [2nd] wiring layer (henceforth the 2nd wiring layer) by the 1st. Layer [1st] aluminum wiring layer (1AL) is chosen as an example as this 2nd wiring layer. It is thin with 40% of the former [width of face / each / of the power supply lines 11 and 12 / case / of this drawing] by making these power supply lines 11 and 12 constitute from a 2nd wiring layer. In addition, the wiring width of face of these power supply lines 11 and 12 is unified as usual between the cells from which a kind differs (this example between the NAND cell of drawing 1 , and the NOR cell of drawing 2).

[0020] The contact structure which supplies supply voltage to transistors 1 or 2 differs from the former by using the wiring layer by the side of the upper layer for the 2nd for these power supply lines 11 and 12 conventionally. That is, on the insulating layer which is not illustrated on the source field 7 of PMOS1, the contact pad layer 13 which consists of 2nd polysilicon contest films, for example is arranged, and this is connected source field 7 through 1CNT. This contact pad layer 13 is connected to the aforementioned current supply line 11 by the side of the upper layer through the 2nd contact (2CNT) formed in the insulating layer which is formed on it, and which is not illustrated. Similarly, in the NMOS2 side, between the source field 9 and GND line 12, the contact pad layer 13 intervenes through an insulating layer, respectively, it connects with the source field 9 by the side of a lower layer through 1CNT, and this contact pad layer 13 is connected to the GND line 12 by the side of the upper layer through 2CNT. In addition, Sign SCNT shows the example of the stack contact which 1CNT and 2CNT (s) made the contact pad layer 13 intervene, and repeated among drawing 2 .

[0021] Since the power supply line consisted of [3rd] wiring layers of the lowest layer conventionally, although the field by the side of the lower layer of this power supply line has not used effectively, in this invention, it is having become possible to aim at a deployment of this lower layer side field by making a power supply line constitute from a wiring layer after a two-layer eye. That is, in order to secure distance with the internal signal line 10 of the same hierarchy in conventional drawing 3 and conventional drawing 4 , the contact section (2CNT, SCNT) which has been arranged only inside the power supply lines 11 and 12 is located the power supply line 11 and directly under 12 with this operation gestalt. Moreover, the internal signal line 10 becomes possible [also wiring directly under the power supply lines 11 and 12]

[0022] As usual, especially the standard cell constituted in this way although not illustrated forms much circuit functional block combining a kind based on customer specification at the time of the arrangement wiring, and is input terminal TIN / output terminal TOUT between this cell. It is further connected the optimal using the 2nd-layer aluminum wiring by the side of the upper layer (2AL), the 3rd-layer aluminum wiring (3AL), and --. Moreover, it is raised in a contact plug or a contact pad layer at an upper layer side, respectively, the wiring layer by the side of the upper layer is communalized, and the power supply lines 11 and 12 by which a series connection is carried out within a cell train at the time of cell arrangement are pulled out outside.

[0023] since the power supply lines 11 and 12 are constituted from the internal signal line 10 by the

wiring layer by the side of the upper layer, the cell base ASIC and the standard cell of this operation gestalt can make line breadth thin, lowering a volume resistivity, without changing the volume resistivity of the power supply lines 11 and 12, and or -- can wire the bottom of the power supply lines 11 and 12 in the internal signal line 10, consequently they can carry out [****]-izing of the whole cell area conventionally For example, in the example of drawing 1 and drawing 2 , 60% of the former [line breadth / of the power supply lines 11 and 12], distance with the internal signal line 10 is small with 40 - 50 conventional%, respectively, consequently cell area is reduction-ized about twenty percent. In this cellular structure, it is also possible to pile up the power supply lines 11 and 12 and the internal signal line 10, and the width of face of the power supply lines 11 and 12 can be further shortened depending on the thickness of 1AL, and the further formation of area reduction of 3 - 50 percent in that case is also possible.

[0024] In addition, although the power supply lines 11 and 12 performed the above-mentioned explanation about the case where the wiring layer of a two-layer eye is used, this invention is not limited to this but it is requirements that the wiring layer for signal lines by the side of the upper layer of a power supply line is the external signal line, i.e., the signal line which can carry out automatic wiring, from a power supply line in an internal signal line, using the wiring layer by the side of the upper layer. Therefore, you may make the external signal line exist in a same hierarchy [as a power supply line], or lower layer side. In this case, as for the external signal line concerned, from a viewpoint of flexibility reservation of wiring, it is desirable that a power supply line and abbreviation parallel wire. Moreover, for this external signal line, an input terminal TIN is [a signal-line cash-drawer position and line breadth being decided beforehand, and only arranging a cell like the aforementioned power supply lines 11 and 12, if it is when the cell of the same function is connected continuously for example, and] the output terminal TOUT of a contiguity cell. You may be the composition by which an automatic connection is carried out. Of course, the external signal line by the side of the same hierarchy as this power supply line or a lower layer was not beforehand formed in the cell, and may be made to wire at the time of automatic wiring.

[0025]

[Effect of the Invention] As explained above, according to the cell base semiconductor device and standard cell concerning this invention, cell area can be reduction-ized, securing the flexibility of signal-line connection of cells to some extent. Moreover, the reduction in resistance of a power supply line is possible, and a voltage drop can be made small. Furthermore, the field by the side of the lower layer of a wiring layer can be used effectively. That is, it uses for the formation of area reduction, and also as shown, for example in this operation gestalt, resistance of leading-about wiring of a gate electrode is reduced, or it becomes possible to prepare contact directly under a power supply line.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the pattern view showing the NAND cell concerning the operation gestalt of this invention.
[Drawing 2] It is the pattern view showing the NOR cell concerning the operation gestalt of this invention.
[Drawing 3] It is the pattern view showing the conventional NAND cell.
[Drawing 4] It is the pattern view showing the conventional NOR cell.
[Description of Notations]
1 [-- p type impurity range 4 / -- n type impurity range, 5 / -- 6 A gate electrode, 8 / -- 7 A drain field, 9 / -- A source field, 10 / -- An internal signal line, 11 / -- A supply voltage supply line (power supply line), 12 / -- A GND line (power supply line), 13 / -- A contact pad layer, TIN / -- An input terminal and TOUT / -- output terminal, 1CNT, 2CNT,, SCNT -- Contact.] -- PMOS,

[Translation done.]

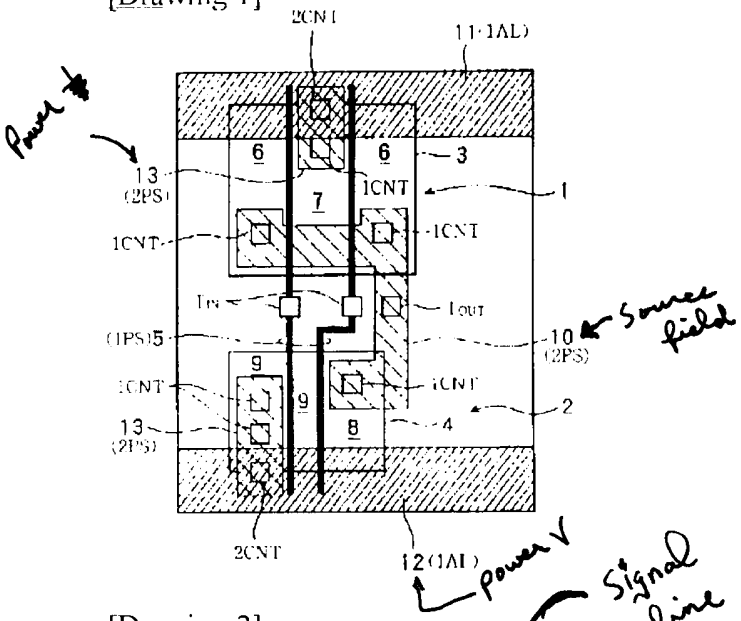
* NOTICES *

Japan Patent Office is not responsible for any damages caused by the use of this translation.

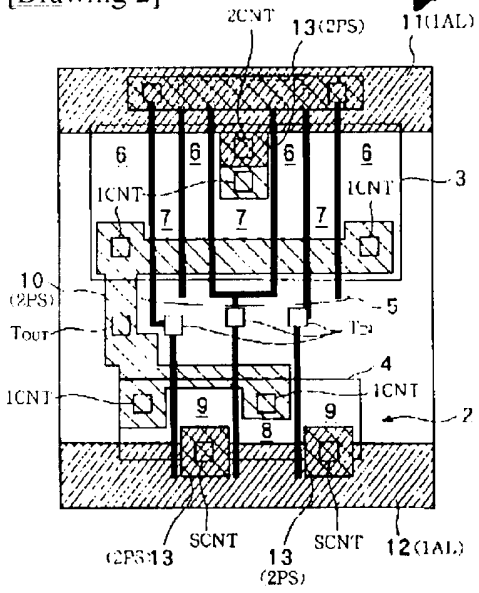
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

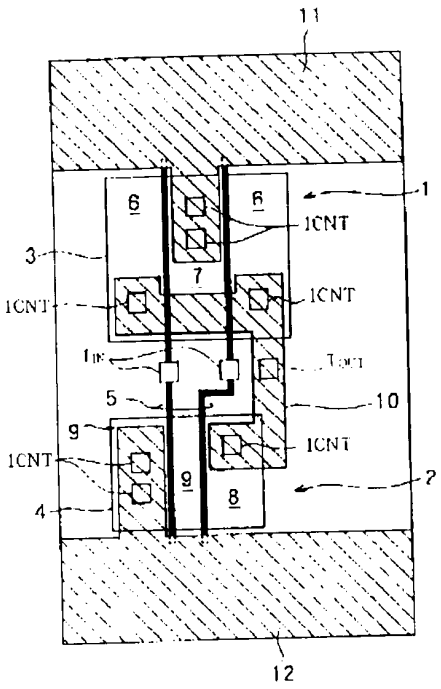
[Drawing 1]



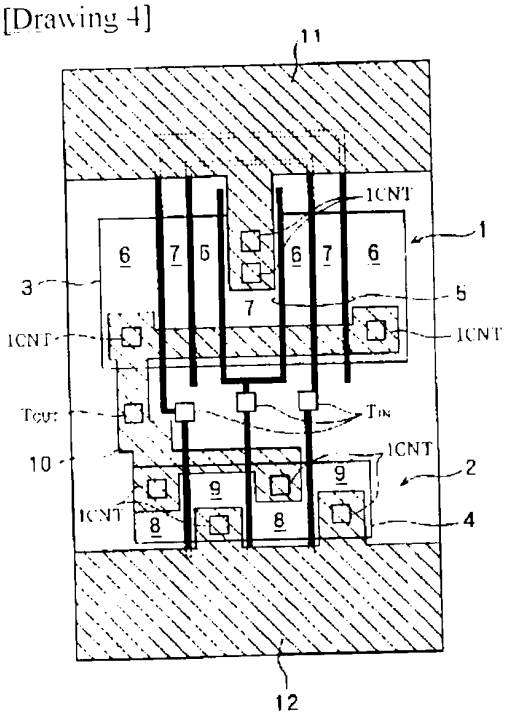
[Drawing 2]



[Drawing 3]



[Drawing 4]



[Translation done.]